

System Specification

Version 1.01

Revision History

Initial Version - Preliminary Version.

1.01 Version - typing correction (2.3 page read : timing unit s->ms correcting)

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1. General

1.1 General Description

a SmartMedia card was used as storage media for a portable device, in a form that can easily be removed for access by a PC. For example, pictures taken with a digital camera would be stored as image files on a SmartMedia card. A user could copy the images to his computer with a SmartMedia reader (typically a small box that connects via USB or some other serial connection).

The SmartMedia card is 2chip 64M(67,108,864)x8bit NAND Flash Memory with a spare 2,048K(2,097,152)x8bit. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation programs the 528-byte page in typically 200s and an erase operation can be performed in typically 2ms on a 16K-byte block. Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verify and margining of data. n, where required, and internal verify and margining of data. Even the write-intensive systems can take advantage of the card extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. a SmartMedia is an optimum solution for large nonvolatile storage applications such as solid state file storage, digital voice recorder, digital still camera and other portable applications requiring non-volatility

1.2 Features of K9F1208U0B

.Single 2.7V~3.6V Supply

.Organization

- Memory Cell Array : (64M + 2,048K)bit x 8bit
- Data Register : (512 + 16)bit x8bit

.Automatic Program and Erase

- Page Program : (512 + 16)Byte
- Block Erase : (16K + 512)Byte

.528-Byte Page Read Operation

- Random Access : 10ms(Max.)
- Serial Page Access : 50ns(Min.)

.Fast Write Cycle Time

- Program Time : 200ms(Typ.)
- Block Erase Time : 2ms(Typ.)

.Command/Address/Data Multiplexed I/O Port

.Hardware Data Protection

- Program/Erase Lockout During Power Transitions

.Reliable CMOS Floating-Gate Technology

- Endurance : 100K Program/Erase Cycles
- Data Retention : 10 Years

.Command Register Operation

.22pad SmartMedia™

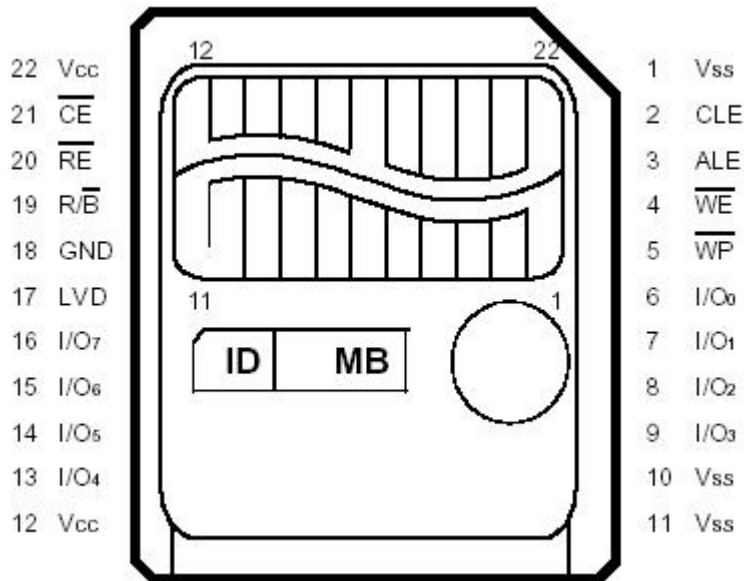
.ID for Copyright Protection

2. Product introduction

2.1 product device

Model No	Capacities	NAND	Availability
SMC-128	128MB	K9F1208U0B*2	Available
SMC-064	64MB	K9F1208U0B	Available

2.2 Pin Description



Note : Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
Do not leave V_{CC} or V_{SS} disconnected.

Pin Name	Pin Function
I/O0 ~ I/O7	Data Input/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{RE}}$	Read Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{WP}}$	Write Protect
LVD	Low Voltage Detect
GND	Ground
R/ $\overline{\text{B}}$	Ready/Busy output
Vcc	Power
Vss	Ground
N.C	No Connection

Command Latch Enable(CLE)

The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE signal.

Address Latch Enable(ALE)

The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE with ALE high.

Chip Enable(CE)

The CE input is the device selection control. When CE goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, CE high is ignored, and does not return the device to standby mode.

Write Enable(WE)

The WE input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE pulse.

Read Enable(RE)

The RE input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE which also increments the internal column address counter by one.

I/O Port : I/O 0 ~ I/O 7

The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.

Write Protect(WP)

The WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP pin is active low.

Ready/Busy(R/B)

The R/ B output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.

Low Voltage Detect(LVD)

The LVD is used to electrically detect the proper supply voltage. By connecting this pin to V_{ss} through a pull-down resistor, it is possible to distinguish 3.3V product from 5V product. When 3.3V is applied as V_{cc} to pins 12 and 22, a 'High' level can be detected on the system side if the device is a 3.3V product, and 'Low' level for 5V product.

2.3 Command sets

K9F1208U0B has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE to low while CE is low. Data is latched on the rising edge of WE Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase command which requires two cycles: one cycle for erase-setup and another for erase-execution after block address loading. The 64M byte physical space requires 26 addresses, thereby requiring four cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table defines the specific commands of the K9F1208U0B.

COMMAND SETS

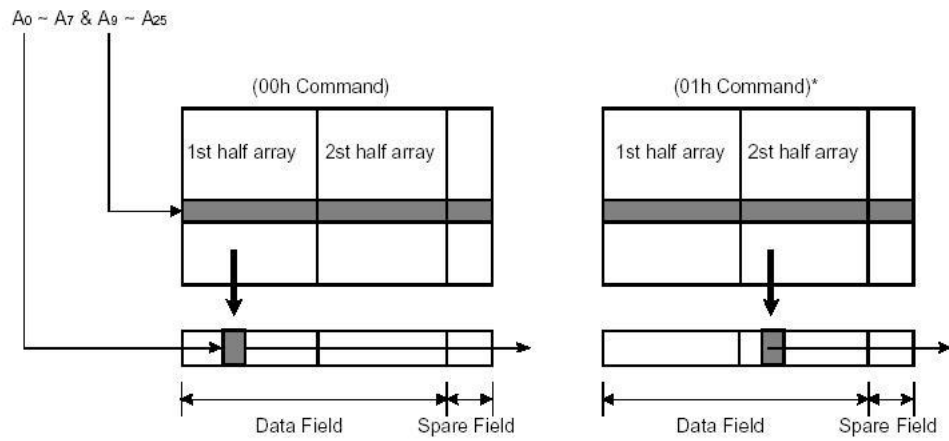
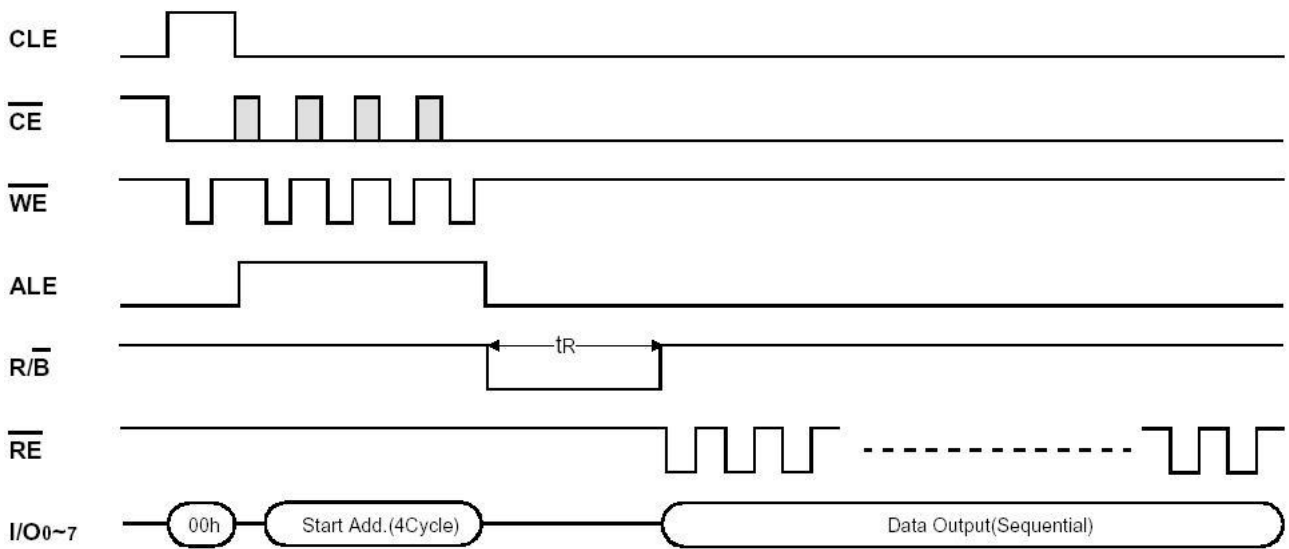
Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h/01h ⁽¹⁾	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	0
Page Program	80h	10h	
Block Erase	60h	D0h	
Read Status	70h	-	0

Note: 1. The 00h command defines starting address of the 1st half of registers.
the 01h command defines starting address of the 2nd half of registers.
After data access on the 2nd half of register by the 01h command, the status pointer is automatically moved to the 1st half 1st register(00h) on the next cycle.

PAGE READ

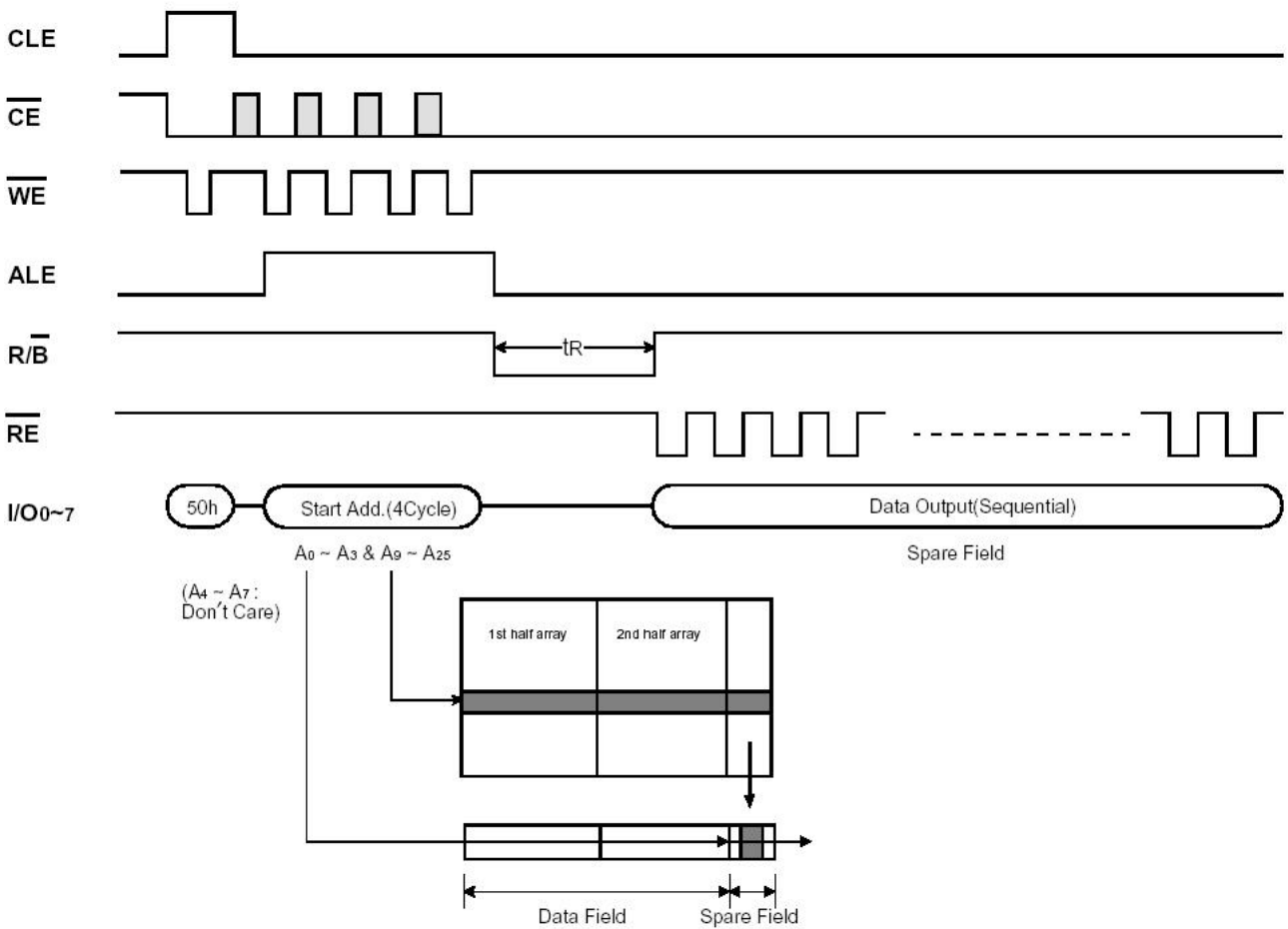
Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with four address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available : random read, serial page read and sequential row read. The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10ms(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing RE High to low transitions of the RE clock output the data starting from the selected column address up to the last column address. After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting 10ms again allows reading the selected page. The sequential row read operation is terminated by bringing CE high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command. Addresses A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read1 operation and spare sixteen bytes of each page may be sequentially read. The Read1 command(00h/01h) is needed to move the pointer back to the main area. Figures show typical sequence and timings for each read operation.

Read1 Operation

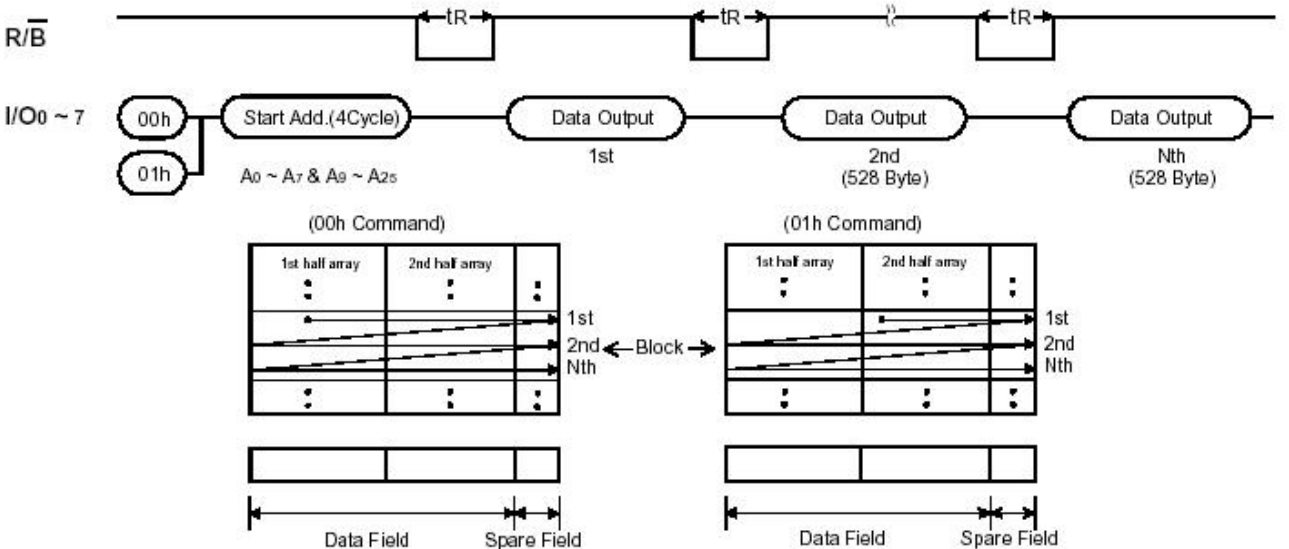


* After data access on 2nd half array by 01h command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

Read2 Operation

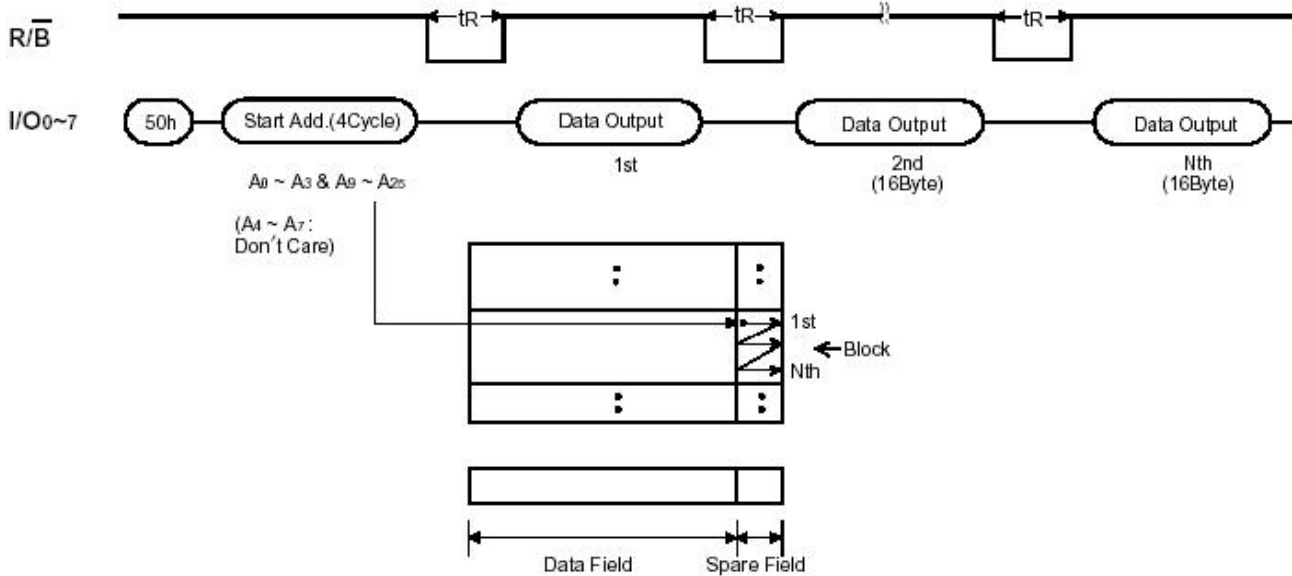


Sequential Row Read1 Operation



The Sequential Read 1 and 2 operation is allowed only within a block and after the last page of a block is read out, the sequential read operation must be terminated by bringing CE high. When the page address moves onto the next block, read command and address must be given

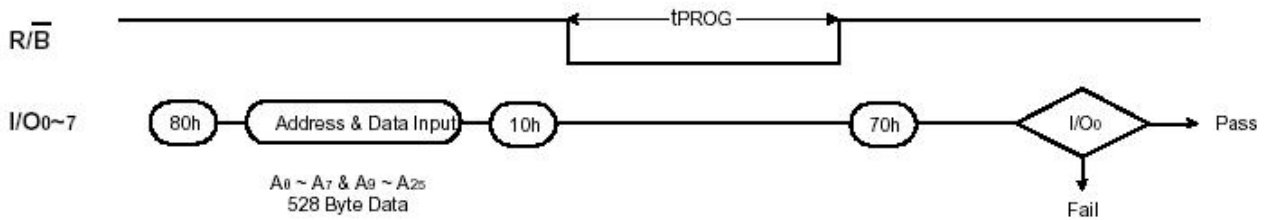
Sequential Row Read2 Operation



PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 for main array and 2 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes. The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the four cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded. The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered, with RE and CE low, to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/ B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

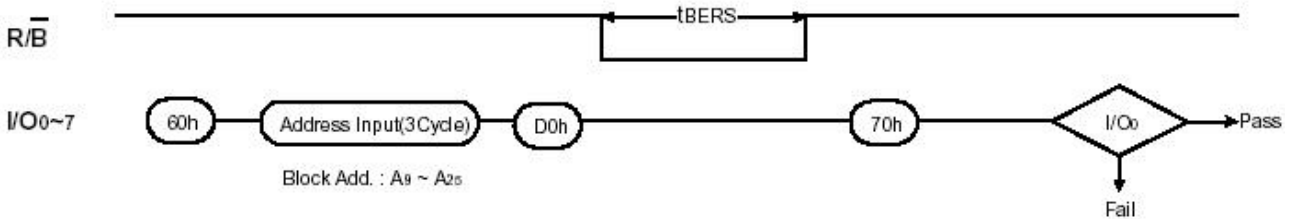
Program & Read Status Operation



BLOCK ERASE

The Erase operation is done on a block(16K Byte) basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only address A14 to A25 is valid while A9 to A13 is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure details the sequence.

Block Erase Operation



READ STATUS

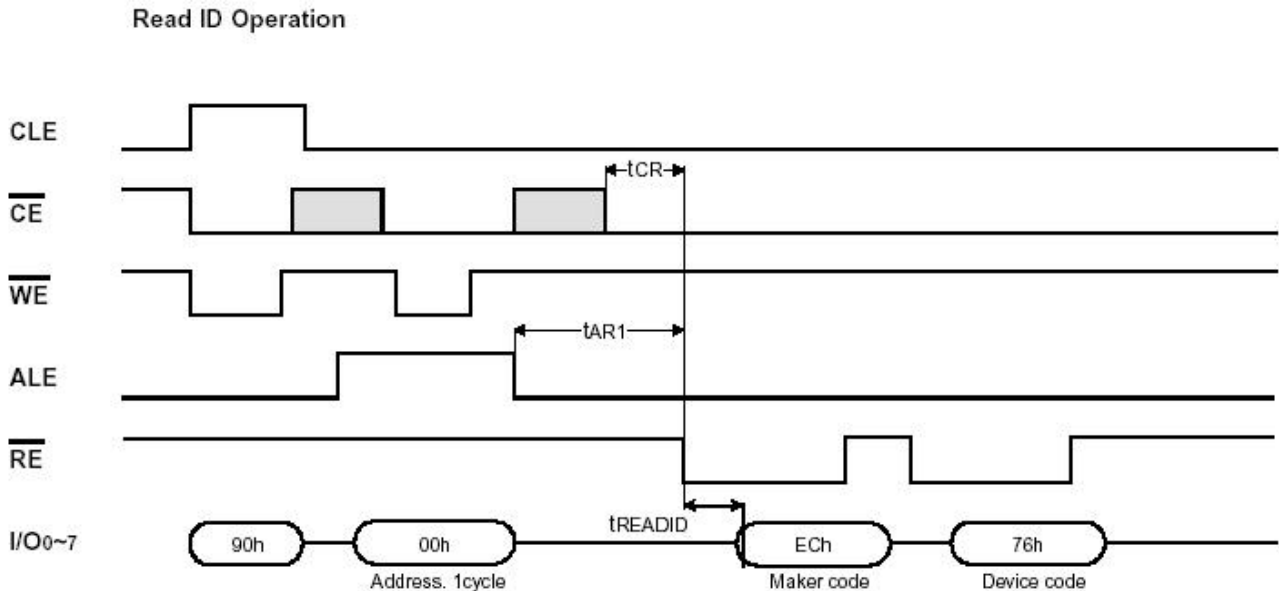
The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE or RE whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. RE or CE does not need to be toggled for updated status. Refer to table 3 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

Read Status Register Definition

I/O #	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program / Erase "1" : Error in Program / Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5		"0"
I/O 6	Device Operation	"0" : Busy "1" : Ready
I/O 7	Write Protect	"0" : Protected "1" : Not Protected

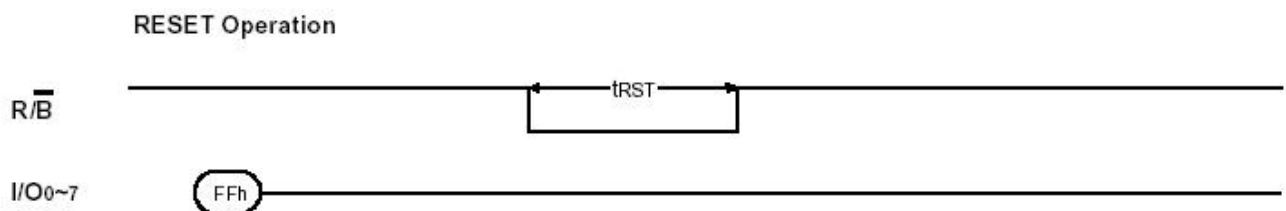
READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code (76H) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure shows the operation sequence.



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 4 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B pin transitions to low for tRST after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure below.



Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

2.4 Electric Characteristics

AC TEST CONDITION

(TA=0 to 55°C, VCC=2.7V~3.6V unless otherwise noted)

Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load (3.0V +/-10%)	1 TTL GATE and CL=50pF
Output Load (3.3V +/-10%)	1 TTL GATE and CL=100pF

CAPACITANCE(TA=25C, VCC=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	C _{IO}	V _L =0V	-	30	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	30	pF

NOTE: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	CE	WE	RE	WP	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input(4clock)
H	L	L		H	H	Write Mode	Command Input
L	H	L		H	H		Address Input(4clock)
L	L	L		H	H	Data Input	
L	L	L	H		X	sequential Read & Data Output	
L	L	L	H	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X ⁽¹⁾	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V _{CC} ⁽²⁾	Stand-by	

NOTE: 1. X can be V_L or V_{IH}.

2. WP should be biased to CMOS high or CMOS low for standby.

Program/Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t _{PROG}	-	200	500	μs
Number of Partial Program Cycles in the Same Page	Main Array	-	-	1	cycle
	Spare Array	-	-	2	cycles
Block Erase Time	t _{BERS}	-	2	3	ms

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE setup Time	tCLS	0	-	ns
CLE Hold Time	tCLH	10	-	ns
\overline{CE} setup Time	tCS	0	-	ns
\overline{CE} Hold Time	tCH	10	-	ns
WE Pulse Width	tWP	25 ⁽¹⁾	-	ns
ALE setup Time	tALS	0	-	ns
ALE Hold Time	tALH	10	-	ns
Data setup Time	tDS	20	-	ns
Data Hold Time	tDH	10	-	ns
Write Cycle Time	tWC	50	-	ns
\overline{WE} High Hold Time	tWH	15	-	ns

NOTE : 1. If tCS is set less than 10ns, tWP must be minimum 35ns, otherwise, tWP may be minimum 25ns.

AC Characteristics for Operation

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	tR	-	10	μ s
ALE to \overline{RE} Delay(ID read)	tAR1	100	-	ns
ALE to \overline{RE} Delay(Read cycle)	tAR2	50	-	ns
\overline{CE} to \overline{RE} Delay(ID read)	tCR	100	-	ns
Ready to \overline{RE} Low	tRR	20	-	ns
\overline{RE} Pulse Width	tRP	30	-	ns
\overline{WE} High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	50	-	ns
\overline{RE} Access Time	tREA	-	35	ns
\overline{RE} High to Output Hi-Z	tRHZ	15	30	ns
\overline{CE} High to Output Hi-Z	tCHZ	-	20	ns
\overline{RE} High Hold Time	tREH	15	-	ns
Output Hi-Z to \overline{RE} Low	tIR	0	-	ns
Last RE High to Busy(at sequential read)	tRB	-	100	ns
\overline{CE} High to Ready(in case of interception by \overline{CE} at read)	tCRY	-	50 +tr(R/B) ⁽¹⁾	ns
\overline{CE} High Hold Time(at the last serial read) ⁽²⁾	tCEH	100	-	ns
\overline{RE} Low to Status Output	tRSTO	-	35	ns
\overline{CE} Low to Status Output	tCSTO	-	45	ns
\overline{WE} High to \overline{RE} Low	tWHR	60	-	ns
\overline{RE} access time(Read ID)	tREADID	-	35	ns
Device Resetting Time(Read/Program/Erase)	tRST	-	5/10/500 ⁽³⁾	μ s

NOTE :

1. The time to Ready depends on the value of the pull-up resistor tied R/B pin.
2. To break the sequential read cycle, \overline{CE} must be held high for longer time than tCEH.
3. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5 μ s.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V _{SS}	V _{IN}	-0.6 to + 4.6	V
	V _{CC}	-0.6 to + 4.6	
Temperature Under Bias	T _{Bias}	-10 to +65	°C
Storage Temperature	T _{STG}	-20 to +65	°C

NOTE:

- Minimum DC voltage is -0.3V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, TA=0 to 55°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V _{CC}	2.7	3.3	3.6	V
Supply Voltage	V _{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Sequential Read	I _{CC1}	t _{RC} =50ns, $\overline{CE}=V_{IL}$, I _{OUT} =0mA	-	10	20	mA
	Program	I _{CC2}	-	-	15	25	
	Erase	I _{CC3}	-	-	15	25	
Stand-by Current(TTL)	I _{SB1}		$\overline{CE}=V_{IH}$, $\overline{WP}=0V/V_{CC}$	-	-	1	μA
Stand-by Current(CMOS)	I _{SB2}		$\overline{CE}=V_{CC}-0.2$, $\overline{WP}=0V/V_{CC}$	-	10	50	
Input Leakage Current	I _{LI}		V _{IN} =0 to 3.6V	-	-	±10	
Output Leakage Current	I _{LO}		V _{OUT} =0 to 3.6V	-	-	±10	V
Input High Voltage, All inputs	V _{IH}		-	2.0	-	V _{CC} +0.3	
Input Low Voltage, All inputs	V _{IL}		-	-0.3	-	0.8	
Output High Voltage Level	V _{OH}		I _{OH} =-400μA	2.4	-	-	mA
Output Low Voltage Level	V _{OL}		I _{OL} =2.1mA	-	-	0.4	
Output Low Current(R/ \overline{B})	I _{OL} (R/ \overline{B})		V _{OL} =0.4V	8	10	-	

2.5 Card Environmental

2.5.1 Environmental performance

- 1) Operating Environmental
Ambient temperature 0°C to 55 °C .
- 2) Storage Environmental
Storage temperature -20°C to 65 °C .

2.5.2 Environmental Resistance

ITEM	TESTING	STANDARD
High Storage Temperature	Test Condition 65°C and 90-95% RH for 96 hours minimum, Vcc=0	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions, including warpage, must conform to the physical use requirements of these specifications after testing. ^(*) ^(*)
Low Storage Temperature	Test Condition -20°C for 96 hours minimum, Vcc=0	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions, including warpage, must conform to the physical use requirements of these specifications after testing. ^(*) ^(*)
High Operating Temperature	Test Condition 55°C for 96 hours minimum, Vcc=Spec.	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions must conform to the physical use requirements of these specifications after testing. ^(*)
Low Operating Temperature	Test Condition 0°C 96 hours minimum, Vcc=Spec.	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions must conform to the physical use requirements of these specifications after testing. ^(*)
Thermal Shock	Test Condition -20°C to 65°C 30 minutes / 100 Cycles, Vcc=0	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions, including warpage, must conform to the physical use requirements of these specifications after testing. ^(*) ^(*)
Moisture Resistance	Maximum Temperature 55°C. Minimum Temperature 0°C. Repeat test for 10 cycles 90-95% RH, Vcc=Spec.	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions, including warpage, must conform to the physical use requirements of these specifications after testing. ^(*) ^(*)
Electrostatic Discharge	IEC-1000-4-2 C=150pF, R=330Ω, Discharge ten (10) times on PAD. See <i>Figure 2-1</i> .	Over ±4kV for contact discharge. Over ±8kV for air discharge to surface . SmartMedia to function as specified after test and all non-volatile memory to retain the data stored prior to test.
X-ray Exposure	140kV @5mA Intensity 0.1Gy minimum for 1 hour minimum.	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test.
Ultraviolet Light Exposure	Wavelength 254nm, Intensity 15,000μW/cm ² Exposure time 20 minutes	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test.

(*1) Appearance inspection: No nicks, cracks, or other abnormalities. The external dimensions shall meet the specifications

(*2) Warpage: See Method of Measuring Warpage.

2.6. Mechanical Performance

Mechanical Performance

ITEM	TESTING	STANDARD
Vibration and High Frequency	Peak at 147m/s^2 (15G) or amplitude of 1.52 mm, at 10Hz to 2,000Hz, 36 cycles for three(3) axes 12 cycles per axis (12hours).	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions must conform to the physical use requirements of these specifications after testing. (*)
Shock	Acceleration 490 m/s^2 Duration 11ms Semi-sine wave	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions must conform to the physical use requirements of these specifications after testing. (*)
Bend Test	Dislocation caused when a load of 11.76N(1.2kgf) is applied. The dislocation shall not exceed 3mm lengthwise and 1mm widthwise. 250 times in each of four(4) directions (30cycles per minute).	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions must conform to the physical use requirements of these specifications after testing. (*)
Drop test	Drop SmartMedia™ two (2) times in three(3) mutually exclusive axes for a height of 75cm onto a noncushioning, vinyl-tile surface.	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions must conform to the physical use requirements of these specifications after testing. (*)
Torque test	Inclination caused when a torque of 0.1568N-m(1.6kgf-cm) is applied. The inclination shall not exceed $\pm 10^\circ$ lengthwise. 1,000 times (30 times per minute)	SmartMedia™ to function as specified after test and all non-volatile memory to retain the data stored prior to test. The form and dimensions must conform to the physical use requirements of these specifications after testing. (*)

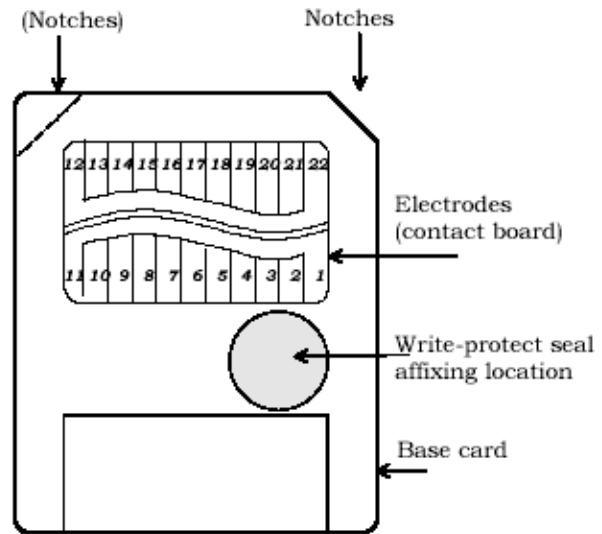
(*) Appearance inspection: No nicks, cracks, or other abnormalities. The external dimensions shall meet the specifications.

3. Card Physical

3.1 card configuration

Part Names

- 1) Electrodes (contact board)
- 2) Notches
- 3) Base card
- 4) Write-protect seal affixing location



3.2 Card Physical Specifications (3.3V 2Chip SmartMedia)

